PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-259306
(43)Date of publication of application : 08.10.1993

(51)Int.Cl. H01L 23/12

(21)Application number : 04-053311
(22)Date of filing : 12.03.1992

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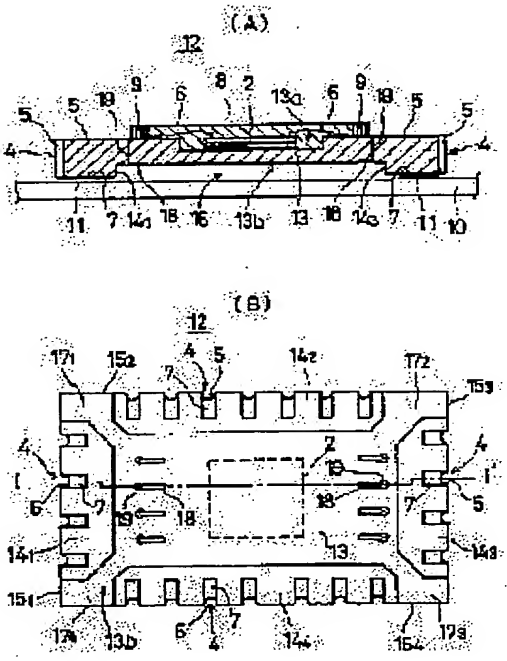
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To enable the cleaning of the circuit board at the bottom of a device and see to that it does not prevent the high integration of the circuit board without increasing the dimension of a package even if the number of terminals increases, concerning a semiconductor device wherein the package on two or more faces of which terminals are arranged is mounted in parallel with the circuit board.
CONSTITUTION: Step parts 141, 142, 143, and 144 are arranged on the bottom 13b of a semiconductor device 12, and space 16 commutating with the outside of a base 3 is made between an outer circuit board 10 and the bottom 13b. A semiconductor chip 2 leads to the circuit board 10 through conductive members 5 and 7. A terminal 17 for test communicating with the semiconductor chip 2 is provided further at the bottom 13b.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Japanese Patent Publication Laid-Open No. 05-259306

[Claim(s)]

[Claim 1] So that the base (13) and the end in which a semiconductor chip (2) is laid may be electrically connected with this semiconductor chip (2) and the exterior of this base (13) and the flow of the other end may be attained In the semiconductor device possessing the conductive member (5 7) arranged in two or more lateral surface (151,152,153,154) of this base (13) So that an external circuit substrate (10) and a flow of this other end (7) of this conductive member (5) may be possible Between the bases (13b) which counter this external circuit substrate (10) and this external circuit substrate (10) of this base (13) in contact with this external circuit substrate (10) when this base (13) is arranged in this external circuit substrate (10) The semiconductor device characterized by providing the step (141,142,143,144) prepared by projecting from the base (13b) of this base (13) so that the outside of this base (13) and the opening section (16) open for free passage might be constituted (12).

[Claim 2] So that the base (13) and the end in which a semiconductor chip (2) is laid may be electrically connected with this semiconductor chip (2) and the exterior of this base (13) and the flow of the other end may be attained In the semiconductor device possessing the conductive member (5 7) arranged in two or more lateral surface (151,152,153,154) of this base (13) On the base (13b) which counters this external circuit substrate (10) of this base (13) when this base (13) is arranged in this external circuit substrate (10) so that an external circuit substrate (10) and a flow of this other end (7) of this conductive member (5) may be possible The semiconductor device characterized by providing further the terminal for a test (18) with which it connects with this semiconductor chip (2) electrically, and the exterior of this base (13) and the flow of the other end of an end are enabled (12).

[Claim 3] Said step (141,142,143,144) is a semiconductor device according to claim 1 characterized by being projected and prepared from said base (13b) of said base (13) which said terminal for a test (18) possesses (12).

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a semiconductor device and relates to the semiconductor device with which a terminal is arranged in two or more fields of a package, and a package is especially mounted in the circuit board by parallel.

[0002] As a result of the number of terminals increasing in recent years with high integration of a semiconductor device, and advanced features, many terminals are arranged in two or more lateral surface of a package possible [an external circuit substrate and a flow], and the semiconductor device with which a package is mounted in the circuit board by parallel is used widely. Since these semiconductor devices miniaturize the circuit board more, what has a small monopoly area on the circuit board is demanded.

[0003]

[Description of the Prior Art] Drawing 2 is the block diagram of an example of the conventional semiconductor device. Drawing 2 (B) is a bottom view and drawing 2 (A) is drawing of longitudinal section in the II-II' line in drawing 2 (B). In addition, drawing 2 R> 2 (A) is LCC (Leadless Chip Carrier). The semiconductor device 1 constituted with a package expresses the condition of having been mounted in the circuit board 10.

[0004] the base 3 consisted of printed circuit board plastics or a laminating ceramic, and is a plate-like configuration, and crevice 3a forms it in a top-face center section -- having -- moreover, lateral surface 151,152,153,154 on all sides **** -- two or more U-shaped gutters 4 (a side notch is called hereafter) are formed, respectively, and the base 3b is made into the flat side. To crevice 3a, a semiconductor chip 2 fixes with adhesives, wirebonding of a semiconductor chip 2 and the metallized layer 5 is carried out with a wire 6, and they are connected. It comes to metalize the front face of the base 3, and the metallized layer 5 is formed by the rim section of base 3b of the base 3 via the inside of the side notch 4 from the top face of the base 3. The pad 7 of an abbreviation rectangle is formed in base 3b of a metallized layer 5.

[0005] A pad 7 is a terminal for soldering at the time of circuit board mounting, and the terminal 11 is arranged at the circuit board 10 corresponding to the location of a pad 7. By applying cream solder to a terminal 11, laying a semiconductor device 1 and carrying out reflow soldering, a semiconductor device 1 is mounted in the circuit board 10.

[0006] since the metallized layer 5 is formed in the side notch 4 at this time -- lateral surface 151,152,153,154 of the base 3 from -- it does not project. Therefore, even if it approaches a semiconductor device 1 on the circuit board 10, it arranges other electrical parts and it contacts, a metallized layer 5 will not short-circuit.

[0007] In addition, when the base 3 is printed circuit board plastics, although a semiconductor chip 2 and a wire 6 are covered with and closed by the sealing agent 8 made of resin, the frame-like lobe 9 is formed in the top face of the base 3 so that a sealing agent 8 may not flow out at this time. Moreover, when the base 3 is a ceramic, the frame-like lobe 9 is formed in the top face of the base 3 as an adhesion side of the cap for sealing crevice 3a which has a semiconductor chip 2.

[0008] By the way, in drawing 2 , since it was easy, the semiconductor device 1 was considered as 22 terminal configurations, but the semiconductor device carrying the LSI (Large Scale Integration) chip which has the logic sections, such as a microcomputer and ASIC (Application Specific Integrated Circuit), has many terminals for I/O signals (I/O terminal), for example, when it is the gate array of the 20,000 gates, the number reaches also near the 300 terminals.

[0009] Moreover, these semiconductor devices have the terminal for much trials besides the terminal for circuit board mounting, and the number of terminals of a semiconductor device tends to increase increasingly with high integration of a semiconductor device, and advanced features in recent years.

[0010]

[Problem(s) to be Solved by the Invention] However, according to the above-mentioned conventional semiconductor device, since base 3b of the base 3 is made flat, in the state of circuit board mounting shown in drawing 2 (A), there is almost no clearance between the front face of the circuit board 10, and base 3b of the base 3. For this reason, in case this is washed after soldering an electrical part to the circuit board 10, it is difficult for a penetrant remover to flow between the front face of the circuit board 10, and base 3b of the base 3, and it was presupposed that this part had been become dirty by residue, such as an activator and flux.

Therefore, when it heat-treats after washing of the circuit board, and the halogen in an activator ionizes, the metallic conductor on the circuit board corrodes, insulation resistance falls, and there is a problem on which the property of the circuit board deteriorates.

[0011] Moreover, since the pad 7 (terminal) for soldering is formed in the rim section of base 3b of the base 3 at a single tier, a semiconductor chip 2 is integrated highly, the number of terminals takes for increasing, and there is a problem which must make a package dimension big according to the number of terminals, and serves as hindrance of the densification of the circuit board even if the dimension of a semiconductor chip 2 is small.

[0012] When it mounts in the circuit board by this invention in view of the above-mentioned point, it aims at offering the semiconductor device which does not serve as hindrance of the densification of the circuit board, without increasing a package dimension to ** even if it can ensure washing of the circuit board, and it does not degrade the property and the number of terminals increases.

[0013]

[Means for Solving the Problem] The above-mentioned problem is solved by constituting as follows.

[0014] Namely, it sets to the semiconductor device possessing the conductive member arranged in two or more lateral surface of the base so that the base and the end in which a semiconductor chip is laid might be connected to a semiconductor chip and an electric target in invention of claim 1 and the exterior of the base and the flow of the other end might be attained. Between the bases which counter an external circuit substrate and the external circuit substrate of the base in contact with an external circuit substrate when the base is arranged in an external circuit substrate so that an external circuit substrate and a flow of the other end of a conductive member may be possible The step prepared by projecting from the base of the base so that the outside of the base and the opening section open for free passage might be constituted was prepared.

[0015] Moreover, in invention of claim 2, the terminal for a test with which an end is connected to a semiconductor chip and an electric target, and the exterior of the base and the flow of the other end are enabled on the base which counters the external circuit substrate of the base when the base is arranged in an external circuit substrate so that an external circuit substrate and a flow of the other end of a conductive member may be possible was further prepared in the above-mentioned semiconductor device.

[0016]

[Function] According to invention of claim 1, when a semiconductor device is soldered to an external circuit substrate, for example and is mounted in it, the opening section is constituted between the bases which counter the circuit board and the external circuit substrate of the base of a semiconductor device, and since this opening section is open for free passage with the outside of the base, it becomes possible for the penetrant remover of the circuit board etc. to flow it into the above-mentioned opening section from the outside of the base.

[0017] Moreover, according to invention of claim 2, this flows with a semiconductor chip and an external circuit substrate, a signal is outputted and inputted, in case the base is arranged on an external circuit substrate, an external circuit substrate and the flowing conductive member are arranged in the lateral surface of the base, on the other hand, it connects with a semiconductor chip and an electric target, and the terminal for a test of the semiconductor chip in which the exterior of **-SU and a flow are possible is arranged in the base which counters the external circuit substrate of **-SU.

[0018]

[Example] Drawing 1 is the block diagram of one example of this invention. Drawing 1 R> 1 (B) is a bottom view, and drawing 1 (A) is drawing of longitudinal section in the I-I' line in drawing 1 (B). In addition, drawing 1 (A) expresses the condition that the semiconductor device 12 constituted with an LCC package was mounted in the circuit board 10. In both drawings, the same sign is given to the same component as the conventional semiconductor device 1 shown in drawing 2 .

[0019] the base 13 consists of printed circuit board plastics or a laminating ceramic, and crevice 13a forms it in a top-face center section -- having -- lateral surface 151,152,153,154 on all sides **** -- two or more side notches 4 form, respectively -- having -- moreover -- the rim section of the four way type of base 13b of the base 13 -- step 141,142,143,144 It is formed. Each step is formed by carrying out cutting of the plate-like four corners and plate-like center section of the base 3 at the bottom which were shown in drawing 2 evenly, and is made flat natural [the base of each step].

[0020] Thereby in the four corners of base 13b of the base 13, it is a step 141,142. It is the inflow path 171 in between. Step 142,143 It is the inflow path 172 in between. Step 143,144 It is the inflow path 173 in between. Step 144,141 It is the inflow path 174 in between. It is formed. Each inflow path is open for free passage through the center section of base 13b of the base 13. Moreover, each inflow path has opening which carries out order amplification on the outside of the base 13 as the graphic display.

[0021] The metallized layer 5 connected with the semiconductor chip 2 by the wire 6 is the step 141,142,143,144 formed in the base of the base 3 via the inside of the side notch 4 from the top face of the base 3. It results and the pad 7 of an abbreviation rectangle is formed in each step of a metallized layer 5, respectively. A pad 7 is soldered to the terminal 11 arranged by the circuit board 10, and a semiconductor device 12 is mounted in the circuit board 10 as shown in drawing 1 (A).

[0022] When the step 141,142,143,144 of base 13b of the base 13 contacts the circuit board 10 in the state of this substrate mounting, the opening section 16 is formed between the circuit board 10 and the base 13. This opening section 16 is the inflow path 171,172,173,174. It minds and is open for free passage with the space of the outside of the base 13.

[0023] Therefore, where a semiconductor device 12 is mounted in the circuit board 10, it is the inflow path 171,172,173,174. It can mind and a penetrant remover can be flowed into the opening section 16 of Hazama of the circuit board 10 and base 13b of the base 13 from the outside of the base 13. For this reason, since the part which becomes the bottom of the base 13 of the circuit board 10 can be washed, even if the metallic conductor pattern is arranged by this part, a metallic conductor pattern does not corrode by heat treatment of a substrate, and the property of the circuit board does not deteriorate, either.

[0024] Moreover, in base 13b of the base 13, it is a step 141. A drawing Nakamigi side and step 143 Two or more terminals 18 for a test are formed in the left-hand side in drawing, respectively. The terminal 18 for a test has flowed with the metallized layer 5 of base 13 top face through the through hole 19 established in base 13b by penetrating from base 13 top face. Since the wire 6 connects with the semiconductor chip 2, the terminal 18 for a test has flowed with the semiconductor chip 2, and, as for a metallized layer 5, can take out the test signal from a semiconductor chip 2 from the terminal 18 for a test.

[0025] Thus, step 141,142,143,144 prepared in the rim section of the base 13 by projecting from base 13b in this example The pad 7 which is a conductive member for outputting and inputting the signal between the circuit board 10 and a semiconductor chip 2 is arranged. Since the terminal 18 for a test which takes out the signal for a test from a semiconductor chip 2 is arranged in base 13b of the base 13, even if the number of terminals increases compared with the conventional semiconductor device which was arranging all

the terminals in the lateral part of the base 13, the dimension of a package is not made large to **. Therefore, there are the features which can contribute to the densification of the circuit board.

[0026] In addition, although this example explained the semiconductor device of an LCC package, a terminal is arranged in two or more fields of a package, and if a package is the semiconductor device of a configuration of that a base, an external circuit substrate, and parallel, i.e., a package, is mounted in contact with a substrate side, it can apply this invention.

[0027]

[Effect of the Invention] When a semiconductor device is mounted in an external circuit substrate like **** according to invention of claim 1, there are the features which can wash the circuit board side which a penetrant remover is made to flow into the opening section constituted by the circuit board and the base base of equipment from the outside of the base, and is located under equipment. Moreover, since according to invention of claim 2 the terminal for a test of a semiconductor chip is arranged in the base of **-SU and only an external circuit substrate and the flowing conductive member are arranged in the lateral surface of the base, there are the features which can be mounted in the circuit board, without enlarging the dimension of the base compared with the conventional semiconductor device.

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of one example of this invention, and drawing 1 (A) is drawing of longitudinal section, and drawing 1 (B) is a bottom view.

[Drawing 2] It is the block diagram of an example of the conventional semiconductor device, and drawing 2 (A) is drawing of longitudinal section, and drawing 2 (B) is a bottom view.

[Description of Notations]

2 Semiconductor Chip

5 Metallizing (Conductive Member)

7 Pad (Conductive Member)

10 Circuit Board

12 Semiconductor Device

13 Base

13b Base

141,142,143,144 Step

151,152,153,154 Lateral surface

16 Opening Section

18 Terminal for Test